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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
FLOURNOY, HORACE L	
ART UNIT	**PAPER NUMBER**
2189	

DATE MAILED: 03/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/786,471	KIM, YOUN-CHEUL	
	Examiner	Art Unit	
	Horace L. Flournoy	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4,6,10,12,14 and 16* is/are allowed.

6)☒ Claim(s) *1-3,5,7-9,11,13 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The instant application having Application No. **10/786,471** has a total of *16* claims pending in the application; there are *3* independent claims and *13* dependent claims, all of which are ready for examination by the examiner.

INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63**.

STATUS OF CLAIM FOR PRIORITY IN THE APPLICATION

As required by **M.P.E.P. 201.14(c),** acknowledgement is made of applicant's claim for priority based on an application filed on February 26, 2003 (Foreign Priority # 2003-11855).

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before

the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 5, 7-9, 11, 13, and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by **Blanc et al. (U.S Patent No. 6,606,300 hereafter referred to as Blanc)**.

With respect to **independent claims 1 and 15,**

"An input/output data pipeline circuit **[Blanc discloses an input/output data pipeline circuit e.g. in FIGs. 2, 3, 11, and column 4, lines 36-37]** *of a semiconductor memory device,* **[disclosed e.g. in FIGs. 2, 3, 11]** *comprising: a control signal generating unit* **[disclosed e.g. in column 2, lines 7-8, 39-41, and 44-46 and in FIG. 11 and associated text.]** *adapted to receive a clock signal and adapted to output a control signal,* **[Blanc discloses in column 37, lines 22-28,"A Phase Acquisition circuit 7212-j receives the GRANT control signal from bus 7131-j and respectively produces a first clock signal 7216-j that is intended for the clock input of latch 7213-j, and produces a second clock signal 7217-j that is used for clocking the second latch 7214-j. To achieve this, the Phase Acquisition circuit 7212-j receives a master clock (MC) signal."]** *a first switching signal, and a second switching signal,* **[see FIGs. 1-5, 11 and 21, and associated text]** *according to a frequency of the clock signal;* **[disclosed, e.g. in column 35, lines 59-61]** *a first transmitting unit* **[FIG. 6, "Switch Core Access Layer (SCAL)" and all associated text]** *adapted to receive data stored in a memory cell and to transmit data to an input/output driver* **[disclosed in column 4, lines 44-51, "The OCD drivers receive the data from**

sixteen routers 3-0 to 3-15 via an associated set of sixteen boundary latches 102-0 to 102-15 (used for timing considerations) so that each router 3-i can retrieve any data located within the 128 locations that are available in Cell Storage 1, and can transport them via a corresponding OCD driver 11-i towards the appropriate destination output port I."] *in response to activation of the first switching signal and the second switching signal;* **[Blanc discloses in column 14, lines 53-55, "FIG. 4 illustrates the use of a single switching module 401 of the present invention in order to provide a switching apparatus." Blanc teaches in FIG. 4 multiple switching signals that can transfer through the switching module 401.]** *and a second transmitting unit* **[FIG. 6, "Switch Core Access Layer (SCAL)" and all associated text]** *adapted to transmit data to the input/output driver in response to activation of the control signal,* **[Blanc teaches the use of multiple transmitting units which anticipate the limitations supra]** *wherein the first transmitting unit and the second transmitting unit are adapted to be alternatively activated."* **[Blanc teaches in FIG. 6 (and associated text) that any number or combination of SCALs can be utilized or activated at a given time through delays. See column 38, lines 8-37]**

With respect to **claims 2, 9, and 15,**

"The input/output data pipeline circuit of claim 1, wherein the first transmitting unit comprises: **[Blanc discloses this limitation, e.g. in the abstract and in column 39, lines 25-60]** *a first switching circuit adapted to output data in response to activation of the first switching signal;* **[see FIGs. 1-5, 11 and 21,**

and associated text] *a latching circuit adaptred to latch and output the output of the first switching circuit;* **[disclosed, e.g. in column 4, lines 41-51]** *and a second switching circuit adapted to output the output of the latching circuit to the input/output driver in response to activation of the second switching signal."* **[Blanc teaches the use of multiple transmitting units which anticipate the limitations supra]**

With respect to **claim 3**,

"The input/output data pipeline circuit of claim 1, wherein the second transmitting unit comprises a third switching circuit, **[this limitation is disclosed, e.g. in column 15, lines 1-10]** *which is adapted to output data to the input/output driver* **[disclosed in column 4, lines 44-51, "The OCD drivers receive the data from sixteen routers 3-0 to 3-15 via an associated set of sixteen boundary latches 102-0 to 102-15 (used for timing considerations) so that each router 3-i can retrieve any data located within the 128 locations that are available in Cell Storage 1, and can transport them via a corresponding OCD driver 11-i towards the appropriate destination output port I."]** *in response to activation of the control signal."* **[disclosed in FIG. 11 and associated text. See column 2, lines 40-46] [Blanc teaches the use of multiple transmitting units which anticipate the limitations supra]**

With respect to **claims 5 and 11,**

"The input/output data pipeline circuit of claim 4, wherein the first switching signal is activated prior to activation of the second switching signal." **[Blanc teaches in FIG. 6 (and associated text) that any number or combination of SCALs can be utilized or activated at a given time through delays. See column 38, lines 8-37]**

With respect to **claims 7 and 15,**

"A semiconductor memory device comprising: a memory cell core, which includes a plurality of memory cells; **[disclosed, e.g. in column 10, lines 48-49]** *an input/output driver adapted to receive first data from outside of the semiconductor memory device,* **[disclosed in column 4, lines 44-51, "The OCD drivers receive the data from sixteen routers 3-0 to 3-15 via an associated set of sixteen boundary latches 102-0 to 102-15 (used for timing considerations) so that each router 3-i can retrieve any data located within the 128 locations that are available in Cell Storage 1, and can transport them via a corresponding OCD driver 11-i towards the appropriate destination output port I."]** *in synchronization with a first clock signal, and adapted to output second data stored in the memory cell core, in synchronization with a second clock signal;* **[this limitation is disclosed in column 38, lines 8-37]** *an input/output data pipeline circuit, which is connected to the memory cell core and the input/output driver,* **[Blanc discloses an input/output data pipeline circuit e.g. in FIGs. 2, 3, 11, and column 4, lines 36-37]** *whcih is adapted to transmit the second data stored in the memory cell core to the*

input/output driver, and which is adapted to transmit the first data received from outside of the semiconductor memory device to the memory cell core; and a control signal generating unit, which is adapted to receive the first clock signal and the second clock signal, and which is adapted to output a control signal corresponding to frequencies of the first clock signal and the second clock signal, wherein the input/output data pipeline circuit includes a first transmitting unit, which which is adapted to perform a transmission operation between the memory cell core and the input/output driver in response to activation of a first switching signal and a second switching signal, **[see FIGs. 1-5, 11 and 21, and associated text. See rejection of claim 1 above]** *and a second transmitting unit which which is adapted to perform a transmission operation between the memory cell core and the input/output driver in response to activation of the control signal, and wherein the first transmitting unit and the second transmitting unit are apated to be alternatively activated."* **[disclosed, e.g. in column 12, lines 35-60 and FIGs. 15 and 21. See also the rejection of claim 1 stated supra]**

With respect to **claim 8**,

"The semiconductor memory device of claim 7, wherein the control signal generating unit which is adapted to detect a phase difference between the first clock signal and the second clock signal, and which is adapted to output the control signal with a logic state based on a detected result." **[Blanc discloses in column 37, lines 22-28,"A Phase Acquisition circuit 7212-j receives the GRANT control signal from bus 7131-j and respectively produces a first**

clock signal 7216-j that is intended for the clock input of latch 7213-j, and produces a second clock signal 7217-j that is used for clocking the second latch 7214-j. To achieve this, the Phase Acquisition circuit 7212-j receives a master clock (MC) signal."]

With respect to **claims 13 and 15**,

"The semiconductor memory device of claim 7, wherein the control signal generating unit **[disclosed in FIG. 11 and associated text. See column 2, lines 40-46]** *is further adapted to receive information about operation modes of the semiconductor memory device, and the control signal corresponds to the first clock signal, the second clock signal, and information about operation modes of the semiconductor memory device."* **[Blanc discloses in column 9, lines 14-19, "Therefore, it appears that the switching module of the present invention permits the sixteen input ports to operate quite independently, that is to say in different modes--either unicast or integrated multicast--in accordance with the contents of the routing header that is being transported by the considered input ports."]**

Allowable Subject Matter

Claims 4, 6, 10, 12, 14, and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

CONCLUSION

Direction of Future Correspondences

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:30 PM (ET).

Important Note

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more

information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Reginald D. Bragdon

REGINALD BRAGDON
PRIMARY EXAMINER

Horace L. Flournoy

Patent Examiner

Art unit: 2189

Supervisory Patent Examiner

Technology Center 2100